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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete If Known	
				Application Number	R53(b) CONT. of S.N. 09/613,138
				Filing Date	March 11, 2004
				First Named Inventor	T. SAITO et al
				Art Unit	2814
				Examiner Name	P. CAO
Sheet	1	of	2	Attorney Docket Number	501.36455CC2

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
PC		US- 4.107.726		08-15-1978	Schilling	
		US- 4.907.066		03-06-1990	Thomas et al	
		US- 4.984.061		01-08-1991	H. Matsumoto	
		US- 5.394.013		02-28-1995	Oku et al	
		US- 5.463.255		10-31-1995	T. Isono	
		US- 5.565.707		10-15-1996	Colgan et al	
		US- 5.659.201		08-19-1997	Wollesen	
		US- 5.691.572		11-25-1997	Chung	
		US- 5.739.579		04-14-1998	Chiana et al	
		US- 5.786.637		07-28-1998	Tabara	
		US- 5.856.707		01-05-1999	Sardella	
		US- 6.181.012		01-30-2001	Edelstein et al	
		US- 6.188.135		02-13-2001	Chan et al	
		US- 6.265.779		07-24-2001	Grill et al	
PC		US- 6.291.885		09-18-2001	Cabral, Jr., et al	
		US-				

[illegible]

Examiner Signature	PHAT X. CAO	Date Considered	9/25/04
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Substitute for form 14498/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	R53(b) CONT. of S.N. 09/613,138
		Filing Date	March 11, 2004
		First Named Inventor	T. SAITO et al
		Group Art Unit	2814
		Examiner Name	P. CAO
Sheet 2 of 2	Attorney Docket Number	501.36455CC2	

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
PC		MAEDA, K., "Semiconductor Manufacturing Equipment Corresponding to the Introduction of New Processes and Materials," Electron Materials, March 1996, pp. 22-27.	
PC		BAI et al, "Copper Interconnection Deposition Techniques and Integration," 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 48-49.	
PC		LICATA et al., "Interconnect Fabrication Processes and the Development of Low-Cost Wiring for CMOS Products," IBM J. Res. Develop., Vol. 39, No. 4, July 1995, pp. 419-435.	

Examiner Signature	PHAT X. CAO	Date Considered	9/25/04
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